RESEARCH STUDY AND DEVELOPMENT OF AN INTEGRATED CIRCUIT

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FOREWORD

The work reported herein was conducted under Program Element 62201F, Project 8952, Task 01.

The final report on Contract AF 40(600)-1188 was prepared by TRW Systems Group, One Space Park, Redondo Beach, California. The principle investigator was Dan J. Dooley, Project Manager. The design and fabrication of 42 experimental telemetry transmitters was conducted by TRW. The evaluation was conducted at AEDC. Final test results were not available to TRW at the time of preparation of this report.

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This technical report has been reviewed and is approved.

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ABSTRACT

The design of a hybrid microminiaturized telemetry unit for use in gun launched projectiles is described. High peak accelerations during launch and short duration flight (2 milliseconds) were two prime considerations during design. The unit was designed and tested at Arnold Engineering Development Center in Ranges K and G of the Von Karman Gas Dynamics Facility. Initial tests indicated that this type of fm telemetry in the 150 mc frequency range would be feasible for aerodynamic measurements.

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ILLUSTRATIONS

ILLUSTRATIONS (Continued)

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1. INTRODUCTION AND SUMMARY

The objective of this program was to design, develop, and manufacture 42 integrated circuit telemetry transmitters. These circuits must be of small enough mass so that they have a reasonable chance of withstanding peak accelerations of 500, 000 g's during average accelerations of 300, 000 g's occurring for approximately 2 msec. The circuits must then be able to transmit pressure and heat transfer information from a projectile. The design philosophy for the integrated circuit, frequency modulated oscillator was based upon three criteria:

a) The circuit configuration must be amenable to microelectronic fabrication

b) The unit must be capable of meeting the required electrical performance

c) The configuration should be of sufficient simplicity that the die size could be minimized and a reasonable yield expected.

Minimizing the die size will ensure a minimum mass which, in turn, improves the possibility of serving and performing under high g loads.

Phase III of this program defined a circuit to meet the design requirements discussed above; however, the circuit was modified to improve performance and ease of fabrication. This final circuit diagram, shown in Figure 1, consists of three circuits: 1) a voltage regulator, 2) an oscillator, and 3) a modulator. The oscillator is a negative resistance, balanced, voltage-stable configuration. This type of oscillator not only meets the design requirements but also provides improved stability performance over other possible circuits. Although the circuit is inherently stable with power supply variations, it was found necessary to incorporate a two-stage voltage regulator in the circuit. This allows the oscillator and modulator to be sensitive to transducer variations yet insensitive to power supply variations. Each portion of the circuit configuration is discussed in detail in the following sections.

The goals that the oscillator was designed to satisfy are listed below. (See Reference 1.)

- Carrier Frequency — 140 MHz $\leq f_c \leq$ 250 MHz
- Full Scale Modulation Bandwidth (FSMB) — >200 KHz

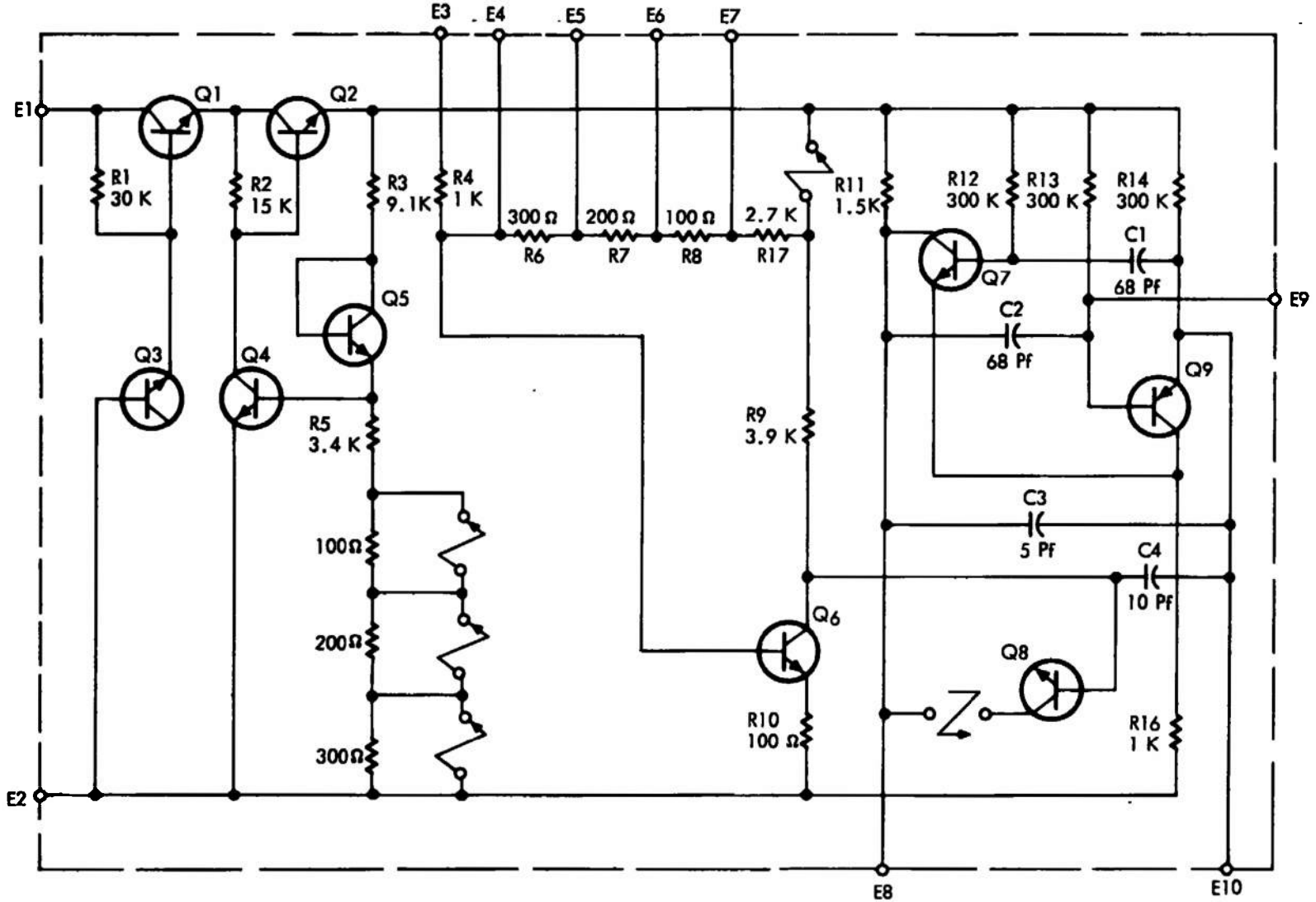


Figure 1 Circuit Configuration of NRO-01

- Frequency stability (2% of FSMB for temperature variations of 2°F) — Max. of 16 KHz
- Signal strength (measured across 50 ohm dipole antenna at 10 ft) — ≥ 75 μV
- Capacitive sensor ΔC for FSMB — ΔC = 0.48 pF
- Resistive sensor ΔR for FSMB — 0.7% of sensor value; 7 ohms for 1 KHz sensor
- Operation for 100 msec from discharge of 200 μF capacitor charged to 9.4 μFV nominal

The antenna would be provided by a single-turn, planar coil. The comparison of the design goals and the performance of the final units show that the goals were met or exceeded by the final 21 units. Sections 4 and 5 discuss the performance and problem areas in detail.

To fabricate the desired circuit configuration in monolithic form, it was necessary to utilize state-of-the-art technology. The realization of the circuit required the use of thin-film capacitors, thin-film resistors, diffused "pinch" resistors, avalanche diode, varicap diode, and high-frequency transistor structures. This is the first time that this variety of components and manufacturing technologies has been combined to form a monolithic integrated circuit. A photomicrograph of a wafer of these circuits is pictured in Figure 2, and the topological layout is shown in Figure 3. The manufacturing technologies necessary to fabricate these units is discussed in Section 3.

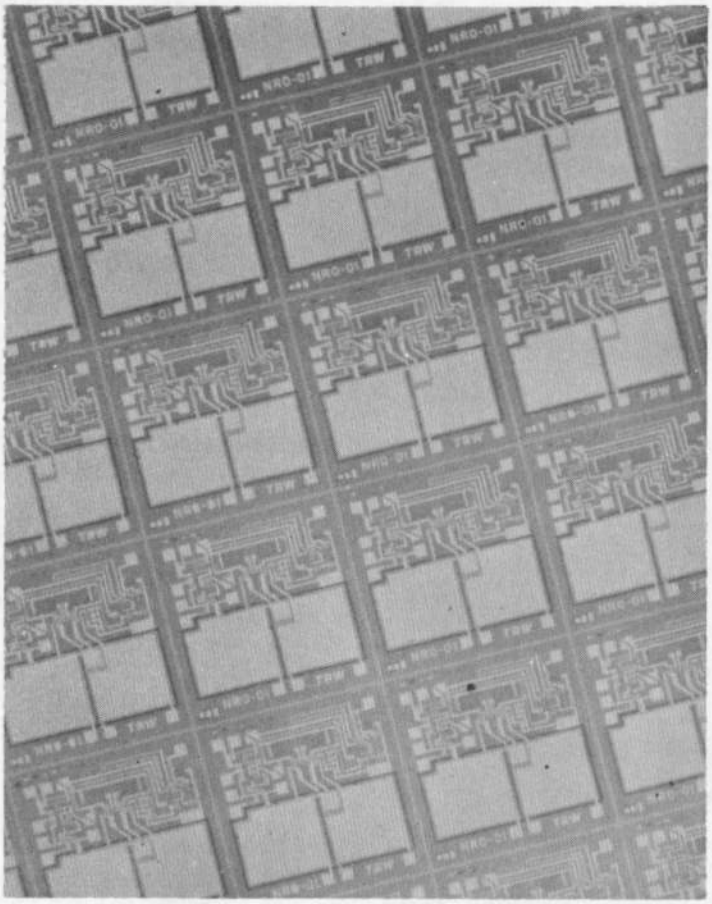


Figure 2 Photomicrograph of Silicon Wafer Containing NRO-01

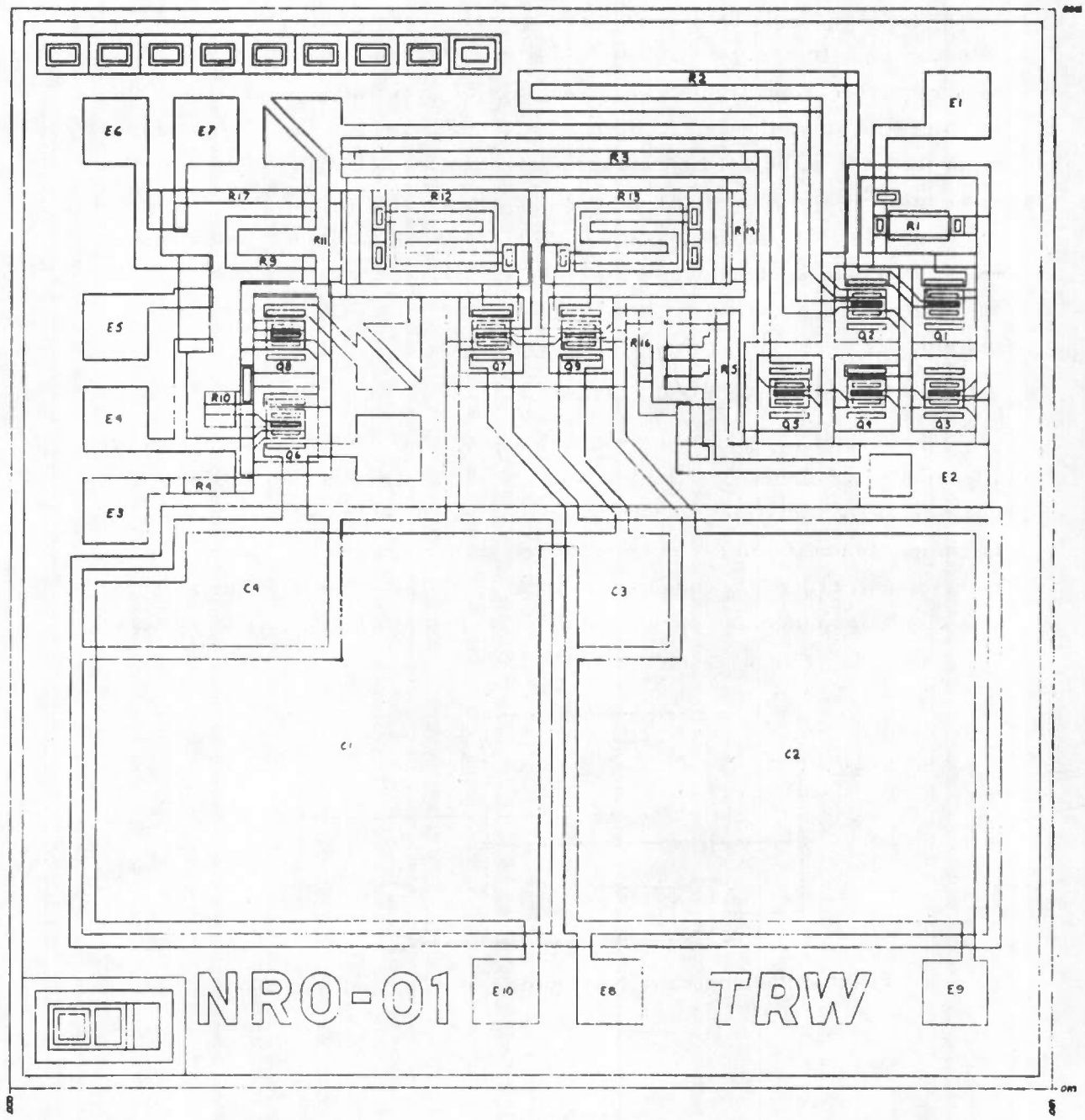


Figure 3 Topological Layout of NRO-01

2. CIRCUIT DESIGN

The design of an oscillator that met the desired performance characteristics was complicated by conflicting design tradeoffs. For example, although high-frequency stability is desired, a large modulation index is also required. Concurrently, a wide range of power supply variations must be tolerated since the unit must operate from a charged capacitor and must meet the desired performance characteristics for 100 msec. Although these requirements complicate the design, the circuit shown in Figure 4 exhibits the desired performance characteristics and is compatible with microelectronic fabrication techniques. To facilitate the understanding of this configuration, the circuit is divided into three parts, which are discussed individually.

2.1 NEGATIVE-RESISTANCE OSCILLATOR

The negative-resistance oscillator (NRO-01) configuration shown in Figure 4 is a balanced, voltage-stable, negative-resistance oscillator and exhibits several distinct advantages over other circuits. First, the circuit is compatible with microelectronic fabrication techniques. The required inductor will utilize the inductance of the specified antenna. This antenna is a single loop of wire approximately 1 in. in diameter. This circuit also

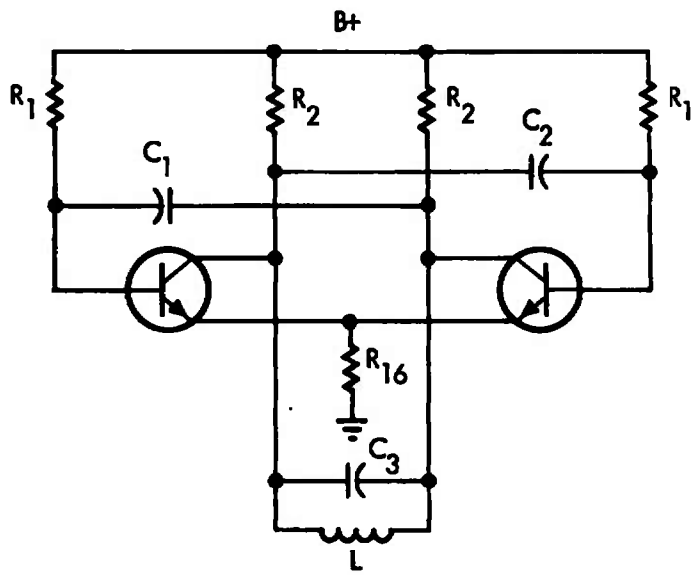


Figure 4 Balanced Negative Resistance Oscillator

exhibits good stability with power supply variations, yet it can be modulated with the required transducers. The requirement that one side of the capacitance transducer remain at ground potential also makes the circuit attractive since the transducer can be connected between either of the two transistor bases and to ground.

The operation of an NRO can be best understood by examining the negative-resistance element shown in Figure 5.

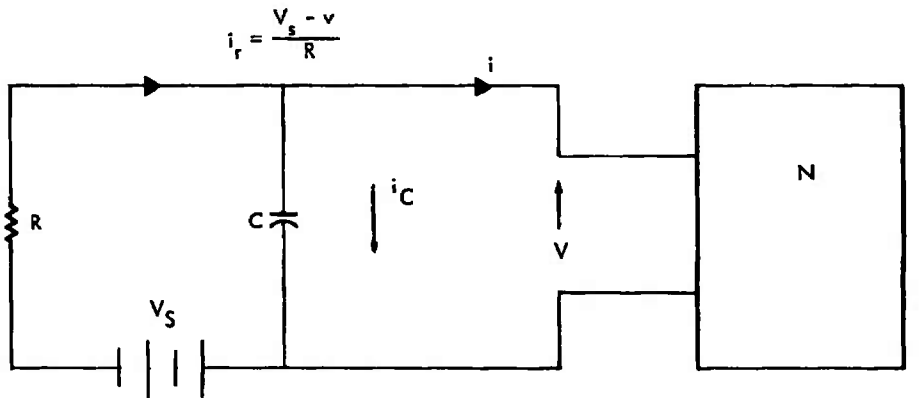


Figure 5 Voltage-Stable Negative Resistance

The following equation may be written by the examination of Figure 5.

$$i_r = i + i_c \tag{1}$$

where

$$i_r = \frac{V_s - v}{R} \tag{2}$$

and

$$i_c = C\frac{dv}{dt} \tag{3}$$

$$\therefore \frac{V_s - v}{R} = i + C\frac{dv}{dt}$$

The i - v characteristic for this circuit is shown in Figure 6.

The current in the three ranges of the negative-resistance characteristic is given by the relationship

$$i = I' + v/R_i \tag{4}$$

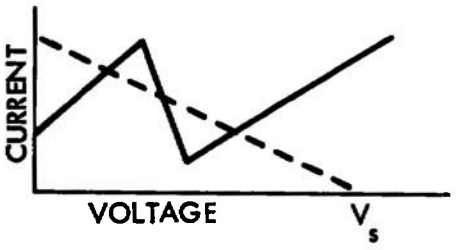


Figure 6 Current Voltage Characteristics of a Voltage-Stable Negative Resistance

where I' is the current at the insection of the current axis by the extension of the corresponding branch of the characteristic.

The NRO now can be configured as shown in Figure 7.

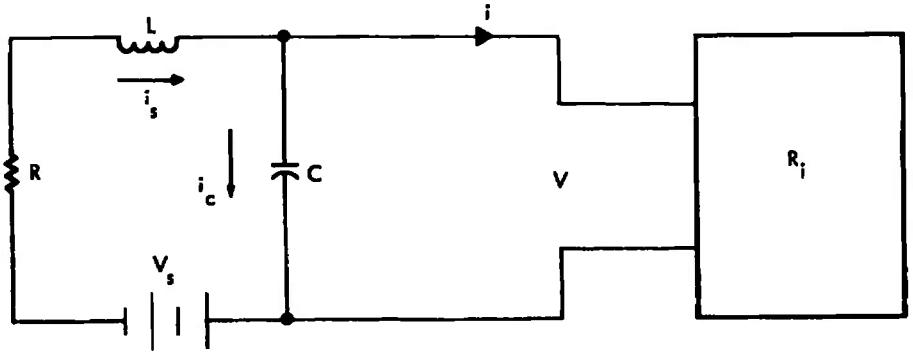


Figure 7 Voltage-Stable Negative-Resistance Oscillator

Using Equation (4) and applying network laws leads to the following differential equation describing network operation:

$$\left[p^2 + \left(\frac{1}{R_i C} + \frac{R}{L}\right) p + \frac{R + R_i}{R_i\, LC}\right] i = \frac{V_s}{RLC} + \frac{I'}{LC} \qquad (5)$$

In this equation, R_i is the reciprocal of the slope of the branch characteristic and p is the time derivative. The solution to this equation can be conveniently written in the form

$$i = Ae^{\lambda t} \sin(\omega t + \theta) + I_o \qquad (6)$$

in which A and θ are arbitrary constants and λ, ω, and I_o are given as follows:

$$\lambda = -1/2 \left(\frac{1}{RC} + \frac{R}{L}\right) \tag{7}$$

$$\omega = \sqrt{\frac{R + R_i}{R_i LC} - \lambda^2} \tag{8}$$

$$I_o = \frac{V_s + I' R_i}{R + R_i} \tag{9}$$

Equations (6) and (7) show that the amplitude of oscillation can either decay to the stable value I_o, be of constant amplitude, or exponentially increase. These conditions can be derived by rewriting Equation (7) in the following form:

$$\lambda = -\frac{1}{2\sqrt{LC}} \left(\sqrt{\frac{L}{C}} \frac{1}{R_i} + \sqrt{\frac{C}{L}} R\right) \tag{10}$$

Thus the dependence of oscillation is

$$\text{decrease} \sqrt{\frac{L}{C}} \frac{1}{R_i} < \sqrt{\frac{C}{L}} R \tag{11}$$

$$\text{constant} \sqrt{\frac{L}{C}} \frac{1}{R_i} = \sqrt{\frac{C}{L}} R \tag{12}$$

$$\text{increase} \sqrt{\frac{L}{C}} \frac{1}{R_i} > \sqrt{\frac{C}{L}} R \tag{13}$$

Because λ is zero when the amplitude of oscillation has reached its equilibrium value, the equilibrium frequency of oscillation is given by Equation (8). This equation can be written more conveniently as

$$\omega = \sqrt{1 - \frac{R^2 L}{C}} \frac{1}{\sqrt{LC}} \tag{14}$$

However, $L/R^2C = Q^2$, and, therefore, Equation (14) becomes

$$\omega = \sqrt{1 - \frac{1}{Q^2}} \frac{1}{\sqrt{LC}} \tag{15}$$

Using a series expansion of $[1 - 1/Q^2]^{1/2}$ and taking the first two terms, Equation (15) is approximately

$$\omega \approx \left(1 - \frac{1}{2Q^2}\right) \frac{1}{\sqrt{LC}} \tag{16}$$

The derivation of this equation is based on the assumption of a linear negative-resistance characteristic. In addition, the frequency of oscillation depends on the effective value of R and, therefore, on the loading of the resonator. As a result, the loading of the modulator circuit (considered below) will have an effect on the frequency of oscillation. It is interesting to note that the frequency of oscillation is independent of R_i (negative resistance) and, therefore, of amplitude and supply voltage. However, a more rigorous analysis in which the curvature of the i - v characteristic in the negative range is considered shows that harmonic generation causes a second-order dependence on supply voltage as well as on the load. This effect can be minimized if the operating point is chosen at a point of inflection in the i - v characteristic. The ability to obtain excellent frequency stability against power supply variations is one of the desirable features of this oscillator configuration.

2.2 MODULATION OF THE NRO

The NRO is modulated by two different types of transducer. The first is a pressure transducer of the capacitance type. $A\Delta C$ in this transducer of 0.6 pF must modulate the oscillator to full-scale modulation bandwidth (FSMB). The second transducer is a resistance type with an approximate value of 1 Ω. $A\Delta R$ = 0.5% absolute value (or 7 Ω) of this transducer must modulate the oscillator full scale. (See Reference 1.) The main tradeoff in modulating the NRO with these transducers is to achieve the desired

modulation bandwidth yet maintain frequency stability with power supply variations and temperature. For the capacitance modulator, the configuration shown in Figure 8 was found to perform satisfactorily.

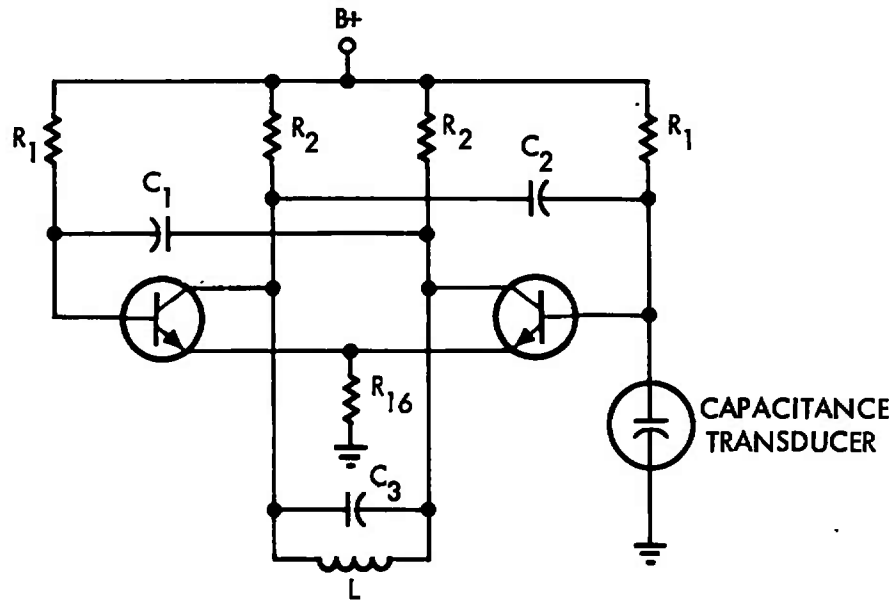


Figure 8 Capacitance Modulated NRO

This modulation is advantageous not only because of the modulation bandwidth achieved (typically 400 KHz), but also because of the lack of proximity effects. The requirement that one side of the capacitance transducer be maintained at ground potential is also satisfied. Over the range of interest, the modulation versus change in capacitance is quite linear.

2.2.1 Modulation with Resistance Transducer

Modulating the NRO with a resistance transducer described in the previous section proved to be a considerable problem. Since a 7-Ω change in the transducer must produce full-scale modulation bandwidth, the oscillator must be made sensitive to these changes. However, this in turn made the oscillator sensitive to power supply variations and temperature.

This task was accomplished by means of a voltage-controlled variable capacitor, a gain stage, and an additional regulator stage to reduce sensitivity to power supply variations. The configuration is shown in Figure 9.

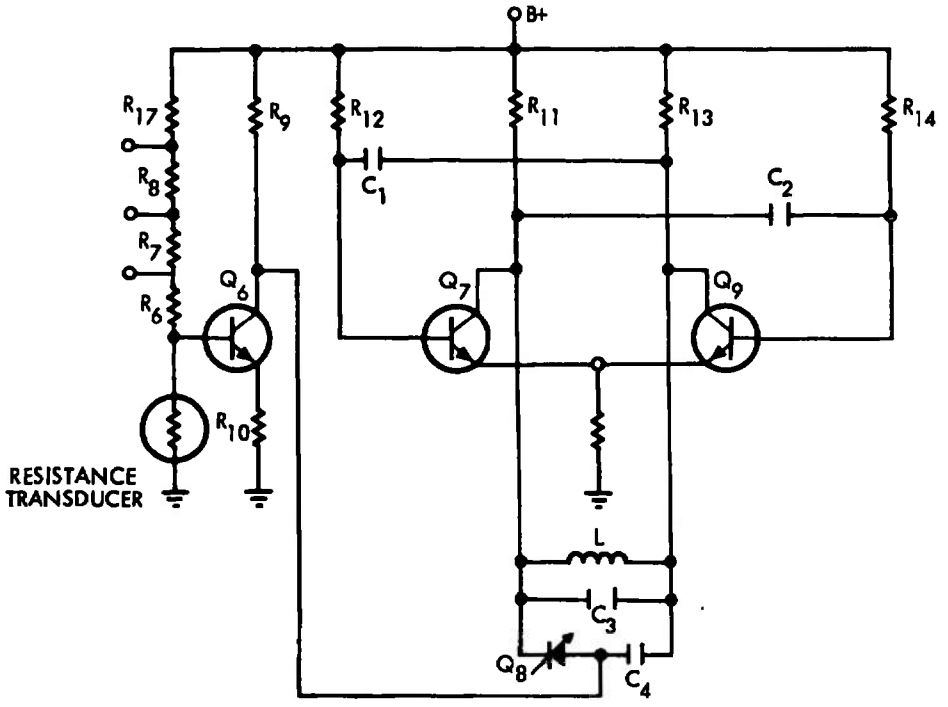


Figure 9 Resistance Modulated NRO

The mode of operation is that a change in resistance of the transducer causes a voltage change at the base of Q_6. This voltage change is then amplified by the common emitter gain-stage Q_6. Subsequently, the voltage appearing across the reverse biased diode Q_8 is changed causing a capacitance to change. The oscillator is modulated because the effective capacitance of the tuned circuit has been varied. This capacitance is the series combination of Q_8 and C_4 in parallel with C_3. Taps are provided on the base resistor of Q_6 to externally adjust the circuit for optimum sensitivity. It was found that the collector base junction provides the best performance

from a sensitivity and linearity viewpoint. Figure 10 illustrates the linearity of this approach. The top curve shows the change in resistance of the sensor versus time with the peak change of 7 Ω. The bottom curve shows the receiver output representing 68 KHz per cm. After the consideration of all the nonlinear elements involved in modulation, transmission, and demodulation, the linearity obtained was not only excellent but exceeded expectations.

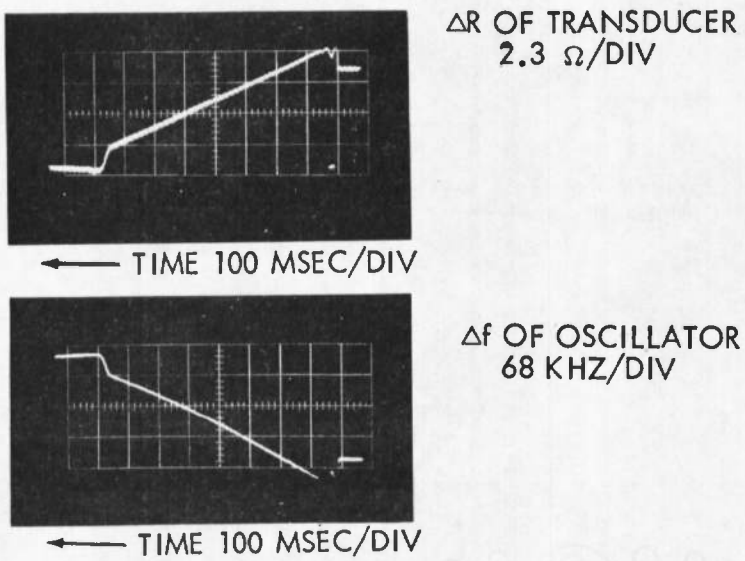


Figure 10 Resistance Modulator Characteristic

2.3 VOLTAGE REGULATOR CIRCUIT

The oscillator is required to meet a frequency stability of 2% FSMB for 100 msec while working from a 200 μF capacitor charged to 9.4 V. (See Reference 1.) This requirement, along with the sensitivity of the oscillator to transducer variations, necessarily increased the performance characteristics required of the voltage regulator. The circuit shown in Figure 11 is the final circuit configuration.

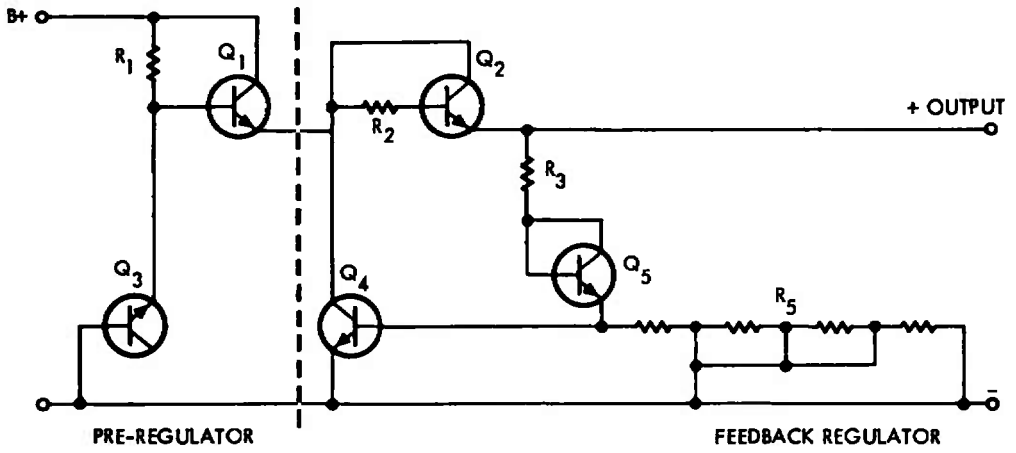


Figure 11 Voltage Regulator Circuit

The design was complicated by the relative low voltage to be regulated (9.4 V) and the dynamic range of the regulator. Basically, the circuit is a series regulator cascaded with a feedback regulator that uses the avalanche breakdown of a transistor emitter-base junction as the reference element. The input voltage is nominally 9.4 V, and the regulated output is 3.0 V. Figure 12 illustrates the output voltage as a function of varying input voltages. The display is read from right to left. From this display, it can be seen that the output varies 1 mV for every 1.2 V change in input voltage. The temperature performance of the regulator is discussed in Section 4.

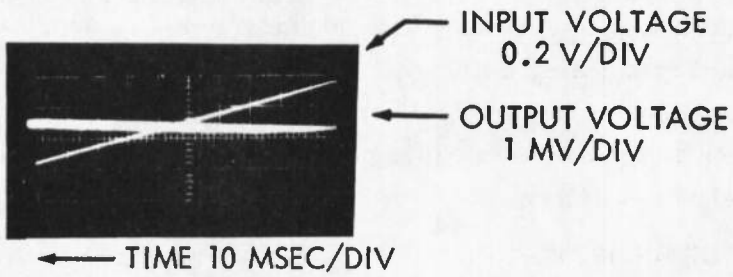


Figure 12 Regulator Input and Output Voltages

3. MICROELECTRONIC FABRICATION

The fabrication of a monolithic VHF oscillator required the use of state-of-the-art processing techniques. To realize the circuit configuration, diffused pinch resistors, thin-film cermet resistors, compatible thin-film capacitors, and double-base stripe, high-frequency transistors were combined into a single monolith. The topological layout of these structures is shown in Figure 3. The die size is 81 x 83 mils and provides approximately 305 possible circuits per wafer. The component design is discussed below in addition to the processing sequence.

3.1 TRANSISTOR DEVICE DESIGN

The device design for the NRO-01 had to include a variety of tradeoffs that reflect component requirements and fabrication controls. These basic tradeoffs can be listed as follows:

a) High transistor f_t at low currents

b) Reasonable transistor current gain at operating bias

c) Compatible diffusions to achieve approximately 10,000 Ω/sq on diffused pinch resistors

d) Compatible transistor characteristics for operating dc regulator, modulator, and oscillator circuits

e) Use of existing fabrication techniques to maintain circuit yield at a reasonable level

f) Emitter-base breakdown compatible with the required avalanche breakdown required in a series regulator.

To perform these tradeoffs in an optimum manner, two computer programs were utilized. Basically, the geometry is fixed; tradeoffs are made with the diffusion profiles; then the geometry is manipulated to yield the final results. The transistor geometry, shown in Figure 13, consists of an emitter and base diffusion into an electrically isolated epitaxial area. This processing technique is illustrated in Figure 14.

The results of these computer programs are shown in Figures 15 and 16. In addition to a listing of the device parameters, a computer plot shown in Figures 17 and 18 illustrates the behavior of current gain and frequency response as a function of bias current. Since the oscillator is

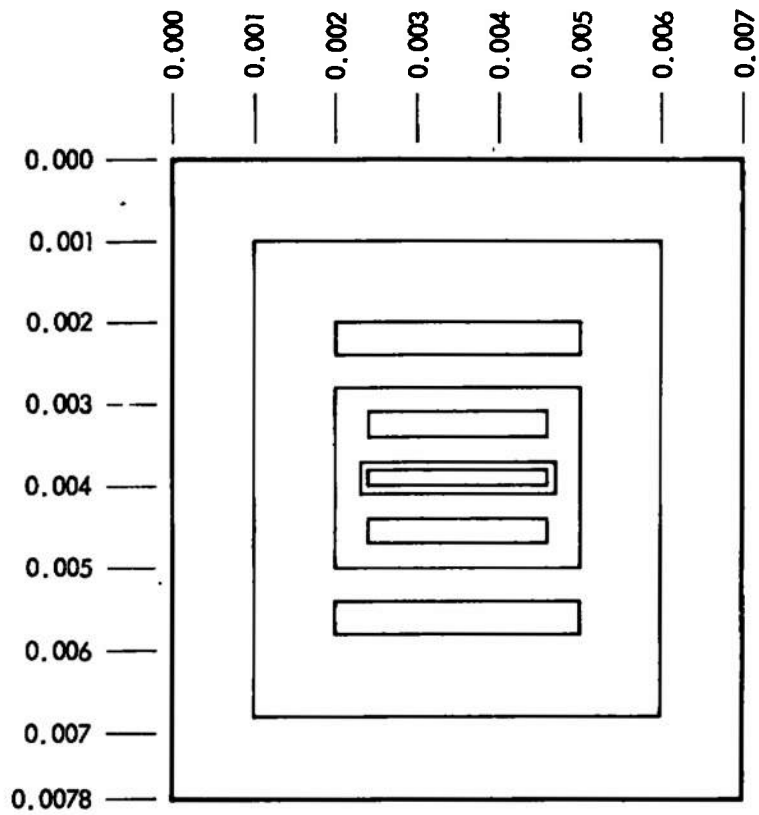
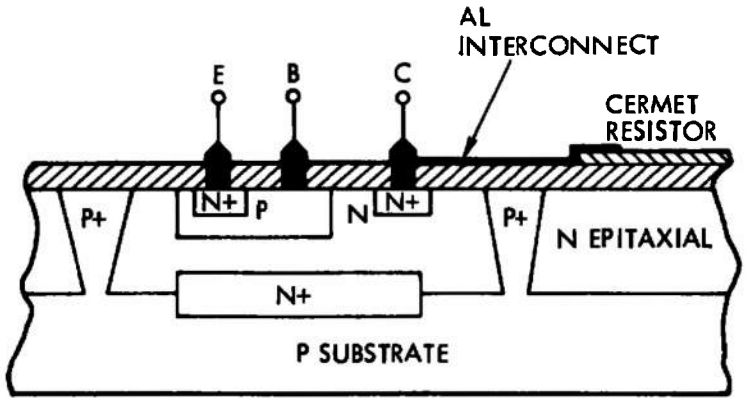


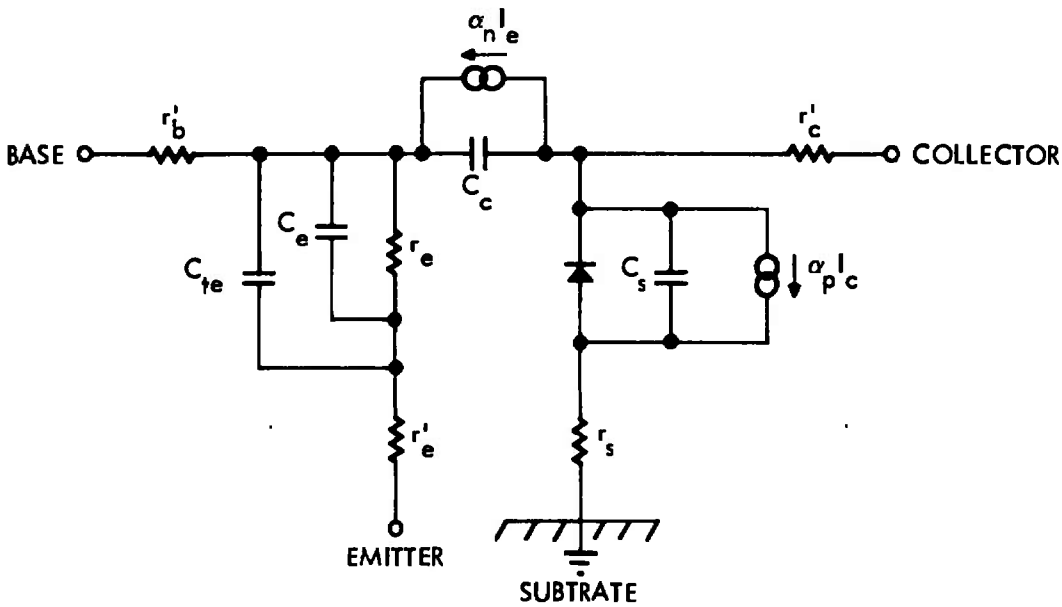
Figure 13 High-Frequency Transistor Geometry

operating at low current (approximately 0.5 mA), it is important to know these parameters.

Because of the parasitics that arise in fabricating a monolithic device, the accurate prediction of performance is not straightforward. Figure 14 illustrates the lumped component equivalent of the parasitics. However, the parasitics are actually distributed in nature. Although this compounds the problem of calculating the performance characteristics, use of the computer programs discussed above have been shown to be accurate whithin the fabrication and process control tolerances.



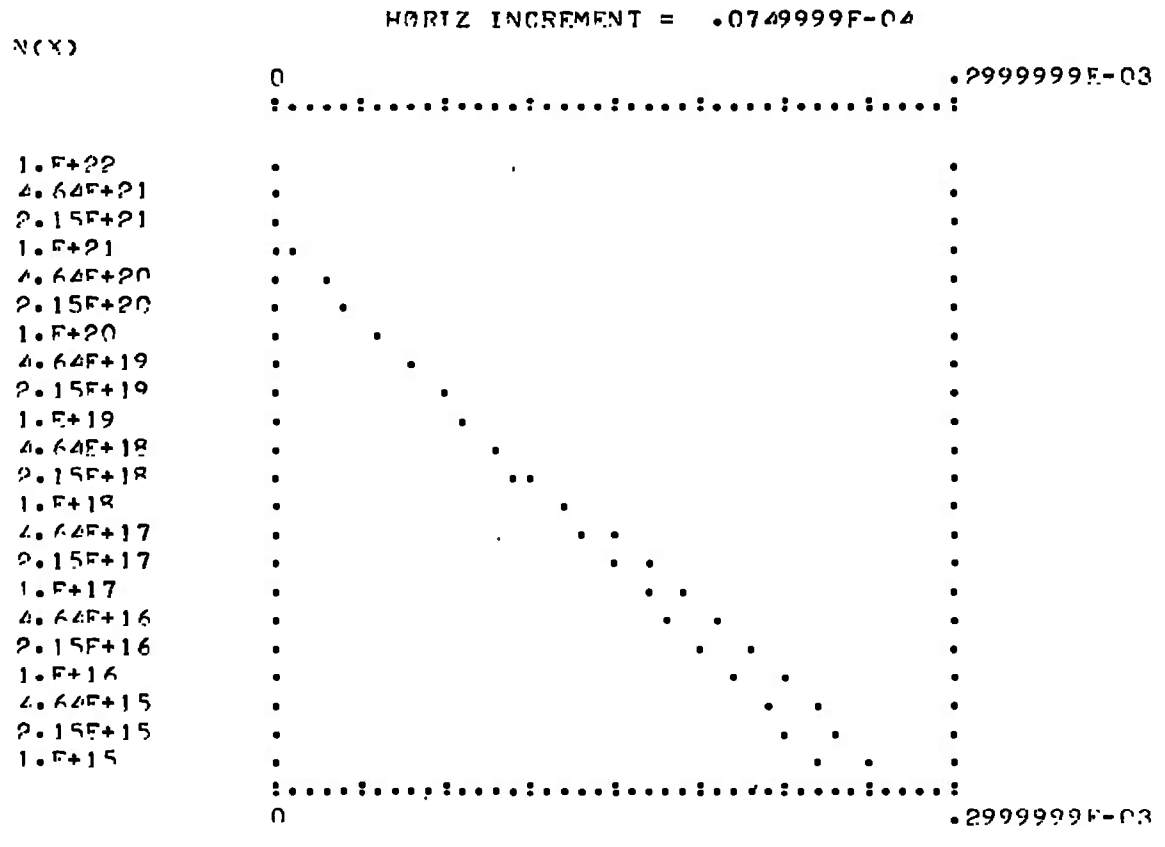
DIFFUSION CROSS SECTION AND STRUCTURE OF
JUNCTION ISOLATED NPN TRANSISTOR



EQUIVALENT CIRCUIT OF JUNCTION
ISOLATED NPN TRANSISTOR

Figure 14 Conventional PN Junction Isolation. Monolithic Device

HIGH FREQUENCY TRANSISTOR



EMITTER-BASE DIFFUSION PROFILE

CARRIER CONCENTRATION OF COLLECTOR	=	1.5E+16
SURFACE CONCENTRATION OF BASE	=	8.6E+18
SURFACE CONCENTRATION OF EMITTER	=	1.5E+21
IMPURITY CONCENTRATION (NB')	=	9.26E+17
AVERAGE CONCENTRATION OF BASE	=	1.6826554E+18
AVERAGE CONCENTRATION OF EMITTER	=	1.9738291E+20
BASE JUNCTION DEPTH	=	.2190522E-03
EMITTER JUNCTION DEPTH	=	.1287676E-03
BASE WIDTH	=	.0902846E-03
BASE DIFFUSION TIME, MIN.	=	20
BASE DIFFUSION TEMP., DEG. C	=	1200
EMITTER DIFFUSION TIME, MIN.	=	10
EMITTER DIFFUSION TEMP., DEG. C	=	1100

Figure 15 Computer Generated Diffusion Characteristics

```
HIGH FREQUENCY TRANSISTOR


          BV(CB0)      =  40.831888    VOLTS
          BV(CE0)      =  14.099166    VOLTS
          BV(EB0)      =  4.6306736    VOLTS
          V(BE)        =  .85839504    VOLTS AT .5E-02   AMPS
          V(CESAT)     =  .13222852    VOLTS AT .5E-02   AMPS
          R(SC)        =  5.8536585    OHMS
          I(CB0)       =  .3760961E-10   AMPS
          H(FE)        =  70.343535    AT .5E-02   AMPS
          ALPHA(-1)    =  .2
          F(T)         =  618.42012    MHZ AT 10   V,  5    MA
          C(S)         =  1.33722  PF AT 10    VOLTS
          C(C)         =  .52965366    PF AT 10    VOLTS
          C(E)         =  7.0057954    PF AT .85   VOLTS
          W(C)         =  10     MICRONS
          W(B)         =  2.19   MICRONS
          W(E)         =  1.29   MICRONS
          R(C)         =  .4     OHM-CM
          RS(B)        =  100    OHM/SQ
          RS(E)        =  2      OHM/SQ

GRADE CONSTANT, BASE:                  8.7006401E+20
GRADE CONSTANT, EMITTER:               3.4409721E+23
DIFFUSION LENGTH, HOLES:               .1092875E-03     CM
DIFFUSION LENGTH, ELECTRONS:           .0674537E-02     CM
DIFFUSION CONSTANT, HOLES:             .23400056     CM SQ/SEC
DIFFUSION CONSTANT, ELECTRONS:         7.8000187     CM SQ/SEC
DEPLETION-LAYER WIDTH, C-B:            .172247E-03   CM
DEPLETION-LAYER WIDTH, E-B:            .0971722E-03     CM
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Figure 16 Computer Analysis of Device Characteristics

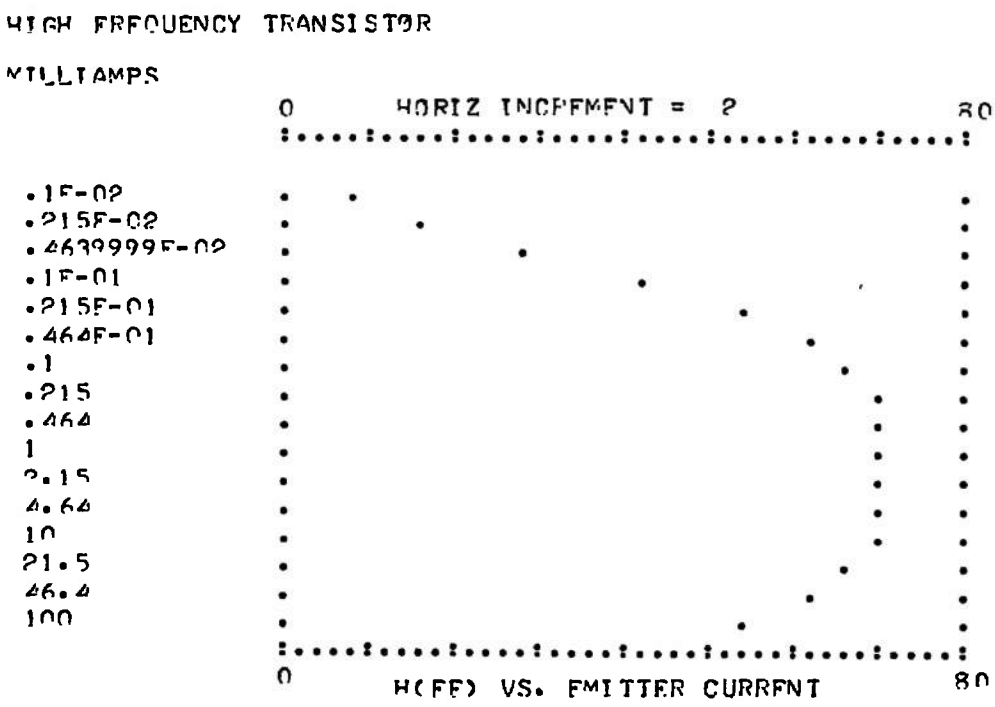


Fig. 17 H(FE) versus Emitter Current

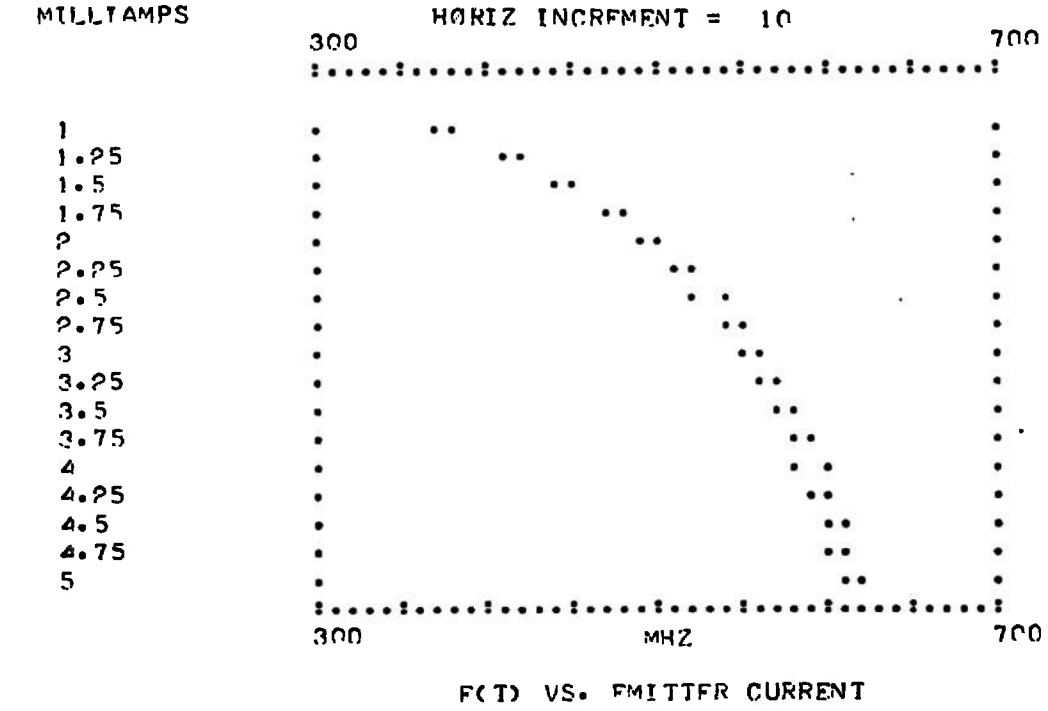


Figure 18 F(T) versus Emitter Current

3.2 DIFFUSED PINCH RESISTOR CHARACTERISTICS

The pinch resistor was used to realize the two large valued resistors in the oscillator circuit and the feedback resistor in the voltage regulator. Basically, this is an ordinary diffused (base) resistor which is reduced in cross-sectional area by making an emitter diffusion on top of it (see Figure 19). The emitter diffusion increases the sheet resistance from the typical 100 to 200 Ω/sq to 10 Ω/sq or higher. Since the area required by other circuit components is large, this technique permits rather large resistors to be fabricated in a relatively small area, thereby alleviating the area problem. There are, however, several limiting characteristics of the pinch resistor. First, it can be seen from Figure 20 that it is linear only for small voltage drops, and it has a low-breakdown voltage (10 V). In addition, the resistor has a large, nonlinear positive temperature coefficient.

Although these deleterious characteristics are troublesome, there are techniques which can be employed to use these characteristics advantageously. In the case of the NRO-01, the nonlinearity of the I-V characteristics is not a problem because only about 2.5 V is across the device. In this region the resistance is quite linear and in manufacturing it has been shown to be quite reproducible. The low-breakdown voltage of the pinch resistor does not present a problem since the circuit prevents more than 4 V from appearing across any of the three pinch resistors. Although the pinch resistor has a high-temperature coefficient, the resistors tend to track with the transistor current gains over temperature. In addition, the matching of identical pinch resistors is nearly as good as diffused base resistors and substantially better than transistor current gains. Therefore, despite the basic limitations of the pinch resistor, it provides adequate performance characteristics for use in the NRO-01.

For the NRO-01 the pinch resistors were designed to have a nominal sheet resistance of 10 kΩ/sq. Although there is some difficulty in accurately controlling this value, a 30% tolerance was observed over a large number of runs.

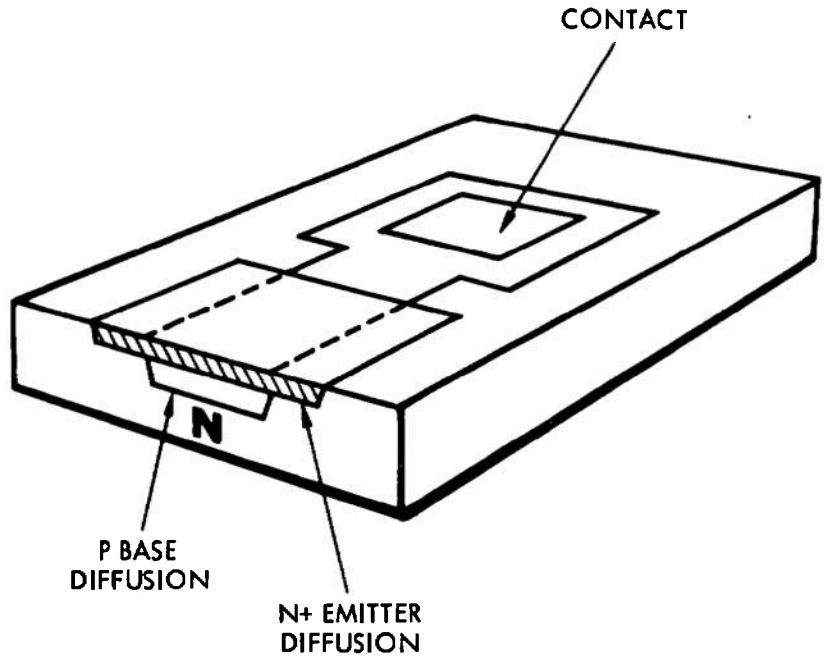


Figure 19 Pinch Resistor Diffused Structure

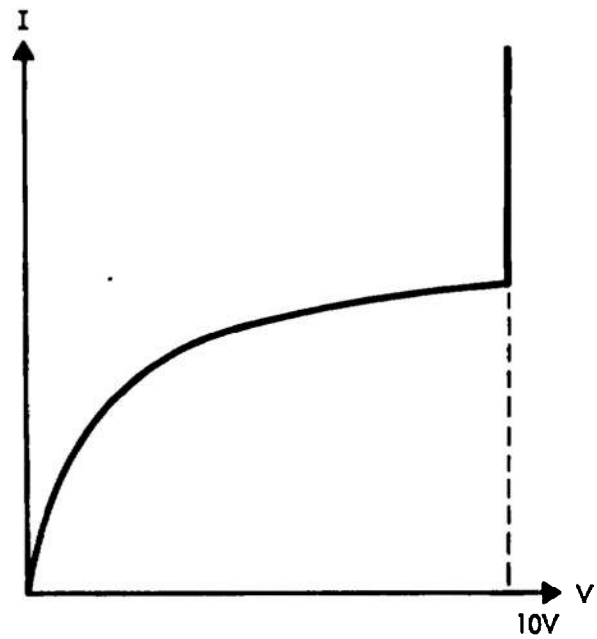


Figure 20 I-V Characteristics of Pinch Resistor

3.3 COMPATIBLE THIN-FILM RESISTORS

In the fabrication of the NRO circuit, thin-film resistors were used for most resistors rather than the conventional diffused, bulk silicon structures. This approach offered advantages in lower temperature coefficients, closer tolerances, and reduced distributed capacitance. The latter characteristic is important when considering the high-frequency operation of the oscillator. The NRO circuit also requires the thin-film resistors that are compatible with chemical and high-temperature processing steps normally associated with monolithic fabrication and packaging techniques. Conventional metal films normally cannot be used for this application without special precautionary techniques. There are, however, resistive films based on metal and ceramic mixtures (cermet) that are nearly impervious to chemical and temperature abuse. The cermet used on the NRO program was the chromium-silicon oxide system formed by flash evaporating a chromium disilicide powder.

Because these films resist most chemical etching reagents, a thin film of aluminum is preferentially etched to define the resistive pattern. After evaporating the cermet film, a suitable aluminum etchant is used to strip the aluminum mask, and thereby leaves the desired cermet pattern (monocarpic technique). The photographic pattern used to define the aluminum mask was designed for a nominal sheet resistance of 300 Ω/sq for the cermet film; however, actual measurements of the resistor line widths were used to modify this value.

Pertinent parameters of the resistive film process and typical characteristics of compatible thin-film resistors are listed below:

Process Parameters

Method	Flash evaporation, $CrSi_2$
Source	Tungsten, 1800°C
Substrate temperature	360°C
Vacuum	$\leq 10^{-5}$ Torr
Sheet resistance	300 Ω/sq, nominal

Electrical Characteristics

Capacitance to substrate	≤ 0.02 pF/mil^2
Breakdown voltage to oxide	≥ 400 V
Leakage current to substrate	$\leq 10^{-9}$ A
Absolute tolerance	±10%
Dissipation	1 mW/mil^2
Temperature coefficient (absolute)	≈ 100 ppm/°C
Temperature coefficient (tracking)	≈ 25 ppm/°C

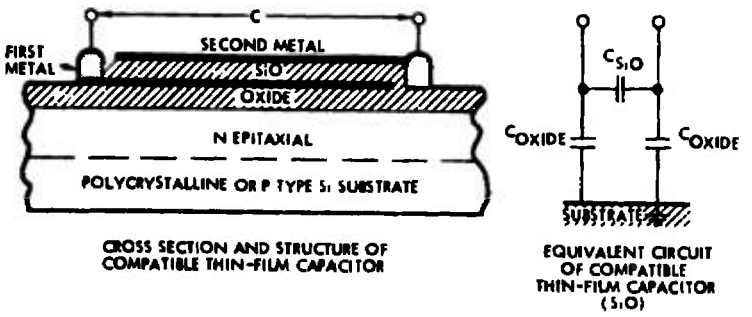
3.4 COMPATIBLE THIN-FILM CAPACITORS

To fabricate the NRO-01, it was necessary to have low-value capacitors with reasonable "Q" factors. This requirement was readily satisfied with silicon monoxide (SiO) thin-film capacitors, which are depicted in cross section in Figure 21. The lower plate is formed during the first aluminum metallization at which time the contacts for the active devices are also formed. Initially in the program, the dielectric (SiO) was deposited through a monocarpic mask (see Subsection 5.1). However, because of several problem areas, a metal or mechanical mask proved to yield the best results. The top plate is then deposited using aluminum to concurrently form the interconnections and bond pads.

Because of the topology of the circuit, the capacitors are also used as crossovers to simplify the layout and minimize the total area required. This area is also reduced by using a common capacitor plate as one large plate for a given connection. Unfortunately, this approach also causes the parasitic capacitance of the large-valued cross-coupling capacitors to be in parallel with the tank capacitor. This in turn lowers the frequency of operation. Typical characteristics observed for the thin-film capacitors fabricated by using monolithic processes are shown below.

Capacitance per unit area	≈ 0.08 pF
Working voltage	≥ 50 Vdc
Dissipation factor at 100 MHz	≈ 0.014

Temperature coefficient (0° to 60°C)	< 50 ppm/°C
Voltage dependence	None
Leakage current at 5 V	$< 10^{-8}$ na
Tolerance	± 10%



CROSS SECTION AND STRUCTURE OF COMPATIBLE THIN-FILM CAPACITOR

EQUIVALENT CIRCUIT OF COMPATIBLE THIN-FILM CAPACITOR (SiO)

$C_{Si,O}$ ~	0.1 pf/mil^2	Id ≤	10^{-9} ma
C_{OXIDE} ≤	0.02 pf/mil^2	TOLERANCE ~	±5% ; ±3% MATCHING
BV ≥	50V	DISSIPATION FACTOR	= 0.01 TO ± 0.1

TYPICAL COMPATIBLE THIN-FILM (SiO) CAPACITOR EQUIVALENT CIRCUIT PARAMETERS

Figure 21 Compatible Thin-Film Capacitor Structure

3.5 FABRICATION SEQUENCE

Because of the complexity and variety of components on the NRO-01, the fabrication techniques and sequence become very important. Basically, the unit is fabricated using planar epitaxial techniques and compatible thin-film depositions. To delineate the geometries of the various device structures, it is necessary to employ eight photographic masks and one mechanical mask. Since the minimum line width is 0.2 mils, it is very important that each mask align with the other masks. The processing steps and fabrication techniques are discussed below.

1) Wafer Preparation. This step initiates the process sequence by polishing three 6-Ω-cm, P-type silicon wafers (1.5 in. diameter). This step is required to ensure a defect-free surface not only to grow the epitaxial layer but also to ensure a proper surface for depositing the thin-film capacitors.

2) First Oxidation. Since SiO_2 is used to mask the silicon substrate from impurity diffusions, this step is necessary to initiate the diffusion sequence.

3) Buried-Layer Diffusion. This diffusion is made to decrease the series collector resistance and reduce the substrate parasitic.

4) Epitaxial Growth. This layer is formed by a chemical reaction between hydrogen gas and silane ($HSiCl_3$) in an epitaxial reactor. A single-crystal silicon layer is then deposited on the silicon wafers, which have been stripped of the masking oxide grown in Step 1. At the same time this layer is grown, it is doped N-type to form the collector regions of the transistors.

5) Oxidation. This oxidation step is required to mask the isolation diffusion.

6) Isolation Diffusion. This diffusion is a P-type diffusion into the N-type epitaxial layer. Upon diffusing through this layer, electrically isolated areas are defined by the two reverse biased diodes formed by this diffusion.

7) Base Diffusion. This P-type diffusion forms the base region of the transistors and the basic diffusion of the pinch resistors.

8) Emitter Diffusion. This N-type diffusion forms the emitter of the transistors and provides the pinch effect for the diffused pinch resistors.

9) Reoxidation. This step consists of not only an oxide growth but also a deposition of ethyl silicate. This additional oxide thickness aids in passivating the surface and decreases the parasitic capacitance associated with components deposited on its surface.

10) Contacts and Beta Adjust. Openings in the oxide are etched to provide contact to the transistors, diodes, and pinch resistors. Probes are used to contact these areas and test junction breakdowns and transistor beta. If the beta is low, the wafers are placed in the furnaces for additional diffusion until a minimum beta of 70 is achieved.

11) Aluminum Monocarpic Deposition. This technique involves the deposition of aluminum to a thickness of 3000 Å. Windows are then etched into the aluminum (down to the SiO_2) in areas where the thin-film cermet resistors are desired.

12) Cermet Resistor Deposition and Definition. The wafers prepared in Step 11 have a cermet film deposited at 300 Ω/sq over the entire wafer. After removal from the vacuum chamber, the remaining aluminum from Step 11 is removed which takes the unwanted cermet with it. Thus, only cermet

deposited through the holes etched into the aluminum remains (monocarpic process).

13) Metal I Aluminum. Aluminum is used to make contact with the active devices and diffused resistors, and it provides the bottom plates of the thin-film capacitors.

14) Silicon Monoxide Deposition (SiO). This material forms the dielectric for the thin-film capacitors. The area into which it is deposited is defined by a mechanical mask which is aligned over the bottom plate metallization.

15) Metallizing Aluminum II. This metallization forms the interconnects and top capacitor plates, and it provides the bonding pads.

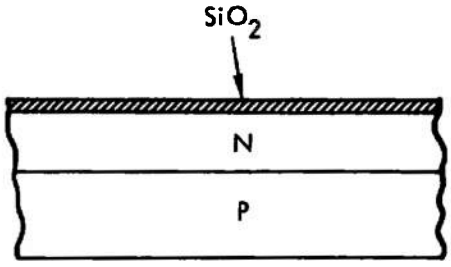
16) Sinter. After Step 15, the wafers are cleaned and heat treated at 540°C to ensure good ohmic contact to devices and to stabilize passive components.

17) Electrical Tests. The wafers are probed to electrically test the circuits for dc voltage and current levels and oscillation. Reject circuits are inked to delineate them from functional units.

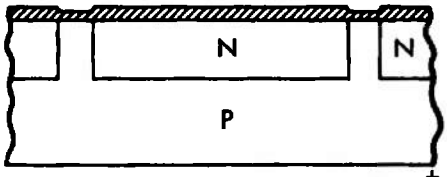
18) Assembly and Test. These straightforward processing steps are listed below:

    a) Scribe and break wafer
    b) Sort dice and clean good dice
    c) Visually inspect good dice at 200X
    d) Mount dice
    e) Wire bond per diagram
    f) Inspect assembled unit
    g) Final-test unit.

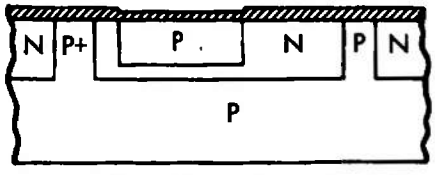
These steps comprise a brief description of the final manufacturing sequence for the NRO-01. As an aid to understanding the manufacturing sequence, Figure 22 illustrates these steps.



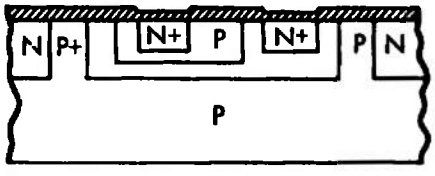
(a) GROW THERMAL SiO_2 LAYER OVER WAFER SURFACE



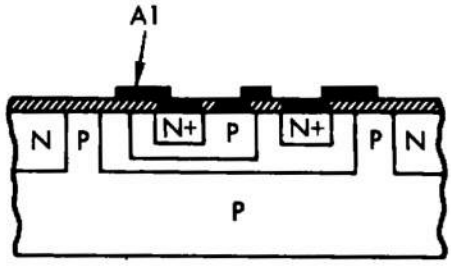
(b) MASK, ETCH, AND DIFFUSE P^+ ISOLATION WALLS, REGROW SURFACE OXIDE



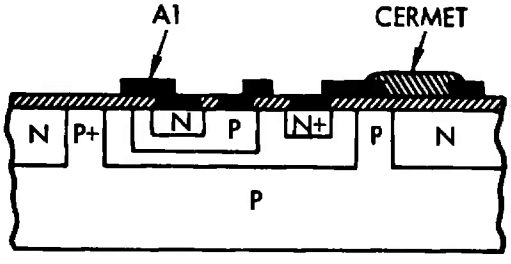
(c) MASK, ETCH, AND DIFFUSE P-TYPE BASE, REGROW SURFACE OXIDE



(d) MASK, ETCH, AND DIFFUSE N^+ EMITTER AND COLLECTOR CONTACTS REGROW SURFACE OXIDE

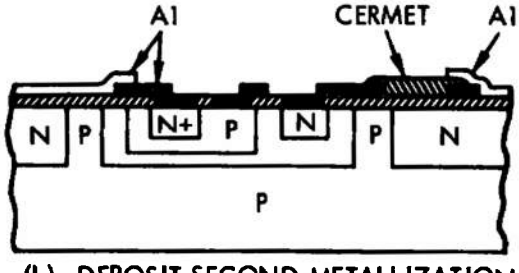


(e) MASK AND ETCH DEVICE CONTACTS. DEPOSIT FIRST METALLIZATION Al FILM, MASK AND ETCH TO DEFINE RESISTOR AND DEVICE CONTACT AREAS AND BOTTOM CAPACITOR PLATES



(f) DEPOSIT THIN-FILM RESISTORS

(g) DEPOSIT SiO DIELECTRIC



(h) DEPOSIT SECOND METALLIZATION Al FILM FORMING INTERCONNECTIONS AND TOP CAPACITOR PLATES.

Figure 22 Integrated Circuit Fabrication

4. CIRCUIT PERFORMANCE OF MONOLITHIC INTEGRATED CIRCUITS

TRW Systems delivered 42 units of the NRO-01 telemetry oscillator to Arnold Engineering Development Center (AEDC) in 10-pin TO-5 packages (see Figure 23). These units were delivered in two groups of 21 units each; the characteristics of the groups are shown in Tables I and II, respectively. The frequency stability was measured by using the test fixtures described in Appendix A; all the units were found to exceed the specification of frequency shifts by less than 2% of FSMB for 100 msec. (See Reference 1.) This is accomplished while working from a 200-μF capacitor charged to 9.4 V. A typical frequency-time characteristic is shown in Figure 24. It is interesting to note that all the units exceeded this specification by at least a factor of two.

One deficiency of the first 21 units delivered to AEDC (see Reference 2) was signal strength. When tested at TRW Systems, all units exhibited a signal strength in excess of the requirement. The design goal was a signal strength greater than 75 μV across a 50Ω dipole antenna located at a distance of 10 ft. (See Reference 1.) However, it was determined that these measurements were in error due to reflections from the walls of the screen room. To correct this measurement error, the second group of 21 units was measured in an area free of metal objects (e.g., cabinets). In addition, the receiver (CEI 501A) was modified to give a digital readout of signal strength and was calibrated with an Empire Singer field strength meter NF105. The resulting measurements, which are shown in Table II, are quite accurate.

The second portion of the signal strength problem was to increase it for the second group of units. By examining the circuit schematic shown in Figure 1, it can be seen that the emitter resistor R_{16} and voltage regulator resistor R_3 can be changed to increase the signal strength. The emitter resistor, R_{16}, can be decreased in value, thus decreasing the emitter degeneration. This approach will account for a major increase in signal strength. Since the frequency stability of the units is several times better than required, lowering this resistance will not cause the units to deviate from the specification. Increasing the value of the resistor, R_3, will also increase the signal strength of the unit; the mechanism for this

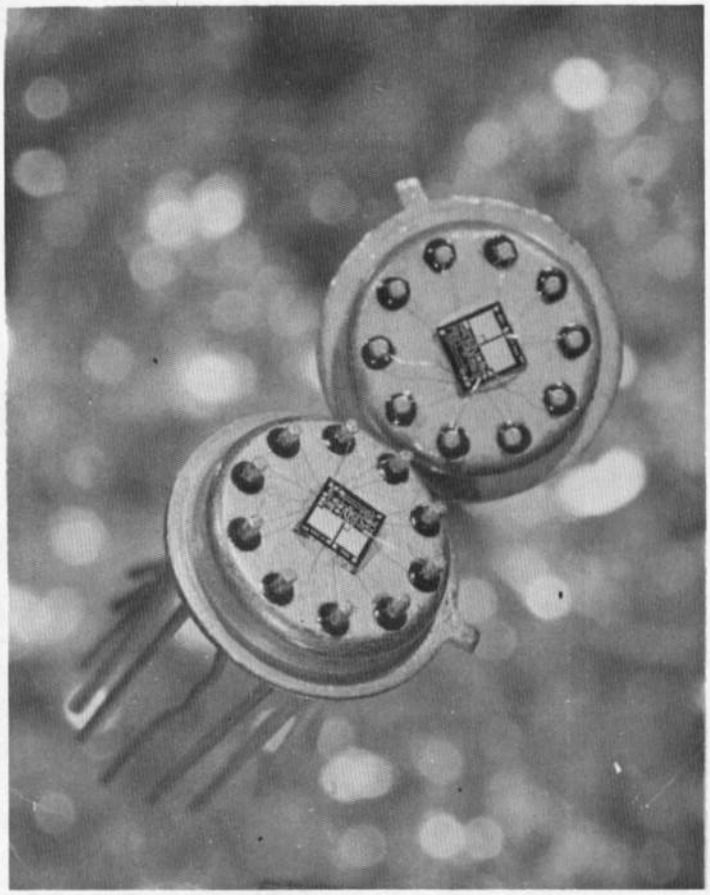


Figure 23 Assembled NRO-01 in 10 Lead TO-5 Package

increase is based on the fact that the change in resistance increases the voltage across the oscillator. This increase in voltage not only permits larger signal swings but also increases the current through the oscillator transistors Q_7 and Q_9. As seen in Figure 17, the f_t is a strong function of current. Increasing the current slightly will then increase the gain and subsequently the signal strength. The units delivered in the second group employed the necessary modifications to ensure meeting the requirements discussed above.

The desired center frequency of operation for the NRO was between 140 and 250 MHz. As can be seen from Table I, the first 21 units did not meet this design goal. (Subsection 5.2 discusses this problem in detail and presents the solution.) It should be noted, however, that the units satisfying Step 3 of the program did meet the center frequency design goal.

Table I. Step II. Test Data for NRO-01

Item	Unit No	Center Frequency	Stability	Signal Strength at 10 Ft	Modulation Bandwidth
1	25	137.5 MHz	<4 KHz at 100 msec	>150 μV	>600 KHz
2	542	126 MHz	<4 KHz at 100 msec	>150 μV	>600 KHz
3	543	130 MHz	<4 KHz at 200 msec	>200 μV	>600 KHz
4	544	131 MHz	<4 KHz at 200 msec	>200 μV	>600 KHz
5	545	132 MHz	<4 KHz at 200 msec	>100 μV	>500 KHz
6	546	131 MHz	<4 KHz at 200 msec	>250 μV	>600 KHz
7	549	130.5 MHz	<4 KHz at 200 msec	>200 μV	>600 KHz
8	550	128 MHz	<4 KHz at 200 msec	>200 μV	>600 KHz
9	551	126 MHz	<4 KHz at 200 msec	>80 μV	>600 KHz
10	555	131 MHz	<4 KHz at 200 msec	>200 μV	>600 KHz
11	556	130 MHz	<4 KHz at 200 msec	>200 μV	>600 KHz
12	557	132 MHz	<4 KHz at 200 msec	>200 μV	>600 KHz
13	560	126 MHz	<4 KHz at 100 msec	>100 μV	>600 KHz
14	561	131 MHz	<4 KHz at 100 msec	>200 μV	>500 KHz
15	563	132 MHz	<4 KHz at 200 msec	>200 μV	>500 KHz
16	566	133 MHz	<4 KHz at 200 msec	>250 μV	>600 KHz
17	567	137 MHz	<4 KHz at 200 msec	>200 μV	>600 KHz
18	568	125 MHz	<4 KHz at 200 msec	>100 μV	>600 KHz
19	570	131.5 MHz	<4 KHz at 200 msec	>200 μV	>600 KHz
20	571	127 MHz	<4 KHz at 200 msec	>75 μV	>600 KHz
21	573	129 MHz	<4 KHz at 200 msec	>200 μV	>600 KHz

Table II. Step III. Test Data for NRO-01

Item	Unit No	Center Frequency	Stability	Signal Strength at 10 Ft	FSMB
1	1	146 MHz	6 KHz at 100 msec	75 μV	>600 KHz
2	2	146 MHz	6 KHz at 100 msec	90 μV	>600 KHz
3	4	143 MHz	6 KHz at 100 msec	95 μV	>600 KHz
4	5	147 MHz	3 KHz at 100 msec	95 μV	>600 KHz
5	6	147 MHz	6 KHz at 100 msec	76 μV	>600 KHz
6	7	146 MHz	6 KHz at 100 msec	75 μV	>600 KHz
7	13	146 MHz	2.8 KHz at 100 msec	75 μV	>600 KHz
8	15	146 MHz	3 KHz at 100 msec	75 μV	>600 KHz
9	19	140 MHz	3 KHz at 100 msec	115 μV	>600 KHz
10	22	140 MHz	7 KHz at 100 msec	75 μV	>600 KHz
11	52	142 MHz	8 KHz at 100 msec	150 μV	>600 KHz
12	53	147 MHz	8 KHz at 100 msec	95 μV	>600 KHz
13	54	145 MHz	6 KHz at 100 msec	95 μV	>600 KHz
14	55	145 MHz	1.5 KHz at 100 msec	88 μV	>600 KHz
15	57	141 MHz	3 KHz at 100 msec	135 μV	>600 KHz
16	59	142 MHz	6 KHz at 100 msec	115 μV	>600 KHz
17	61	140 MHz	3 KHz at 100 msec	95 μV	>600 KHz
18	62	145 MHz	4.4 KHz at 100 msec	80 μV	>600 KHz
19	63	141 MHz	3 KHz at 100 msec	136 μV	>600 KHz
20	64	144 MHz	2.7 KHz at 100 msec	95 μV	>600 KHz
21	65	143 MHz	3 KHz at 100 msec	124 μV	>600 KHz

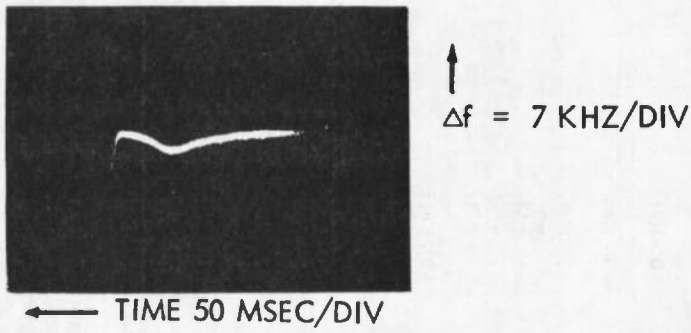


Figure 24 Typical Frequency-Time Characteristic

Arnold Engineering Development Center performed static compression tests on seven units delivered on Step 2 of the contract. After electrical tests were performed, a 0.185-in. diameter hole was drilled in the top of each case and the case filled with an epoxy resin. Subsequent testing indicated no degradation of electrical performance. The units were then potted into static compression test slugs (1.125-in. in diameter by approximately 1.4-in. long) and were statically tested. Load was applied to the slugs in progressive 2000-lb increments and removed completely following each increase in loading. After removal of each increment of load, permanent frequency shifts were recorded. Results of the tests are presented in Table III. The results show that four units ceased to operate after load removal (see Reference 2). The failure was evidently caused by the lifting of a bond wire from the monolithic chip to the TO-5 header since little or no current was being drawn after load removal. To alleviate this problem, all units delivered in Step 3 were double bonded with aluminum wire between the integrated circuit and the header. This approach should increase the possibility of surviving high g loading.

Six units of the NRO-01 were temperature cycled from 15° to 35°C to ascertain temperature performance. The change in frequency was approximately a linear function with temperature exhibiting an average temperature coefficient of 400 ppm/°C. To determine the cause of this TCF, several units were specially bonded to measure the TC of the thin-film capacitors, the individual oscillator circuit, and the voltage regulator. Results of these tests show that the thin-film capacitors have temperature coefficients of less than 50 ppm/°C over the temperature range 0° to 60°C.

Table III. Static Compression Test TRW Monoliths

Circuit Number	Operating Frequency (MHz)	Frequency Shift After Load Removal (KHz)					Comments
		2 K lb	4 K lb	6 K lb	8 K lb	10 K lb	
556	131.5	0	Quit				Quit during load removal. No current.
560	128	Quit					Quit during load removal No current.
568	106	7	30	Quit			Quit at 4.3 K lb external antenna 0.4 mA current drain after test.
570	122	7	21	23	0	-30	External antenna.
573	130	-7	+21	-7	-53	-53	
513	129	0	+20	+60	+17	~400	Still operating after test. Ball bond, gold leads.
535	130	+12	+40	-20	-225	Quit	

This test also showed that the TC of the tank capacitor was not causing the large TCF of the overall telemetry oscillator. When evaluating the individual monolithic oscillator circuits, it was determined that all units had TCF's of less than 45 ppm/^{o}C. This variation in B+ voltage on the oscillator causes the observed TCF of the overall circuit. It is interesting to note that all the units delivered were of the capacitance-modulated type, and that these units exhibit the temperature characteristic discussed above. However, because of the nature of the resistance modulated unit, the TCV of the regulator compensates the resistance modulator leading to overall TCF of the circuit of less than 75 ppm/^{o}C. Recommendations concerning this circuit characteristic are presented in Section 6.

The 42 delivered units illustrate that a monolithic circuit configuration can be realized to produce the desired electrical performance characteristics. Recommended improvements by AEDC were considered and used to produce the characteristics exhibited by the units delivered on Step 3 of the program (see Table II). The minor problems discussed above are understood, and recommendations given in Section 6.

5. PROBLEMS AND SOLUTIONS

The problems in fabricating the NRO-01 can be classified into two areas: first, those problems associated with microelectronic processing, and second, those associated with the resulting circuit performance. The majority of the fabrication difficulties were associated with surface processing, i.e., after the transistors were formed through the interconnect metallization step. Each problem and the resulting solution are discussed in detail below.

5.1 MICROELECTRONIC PROCESSING PROBLEMS AND SOLUTIONS

After the first lot of NRO-01 was completed, it was evident that several problems existed with the interconnect and top capacitor plate metallization. The most evident problem was a masking error which allowed only 0.2 mils between the contact metallization of Q_8, the varicap diode. This spacing is difficult to define in the thick layer of aluminum which forms the interconnects. Another problem existed with this metallization in the connections to the top plates of the capacitors. Since this connection must go over the SiO dielectric step, the metal is quite thin. In addition, the photoresist used to define the connection also thins at this step. The result of this thinning is that the photoresist breaks down during the etching operation causing the metal to be etched through. The spacing problem was alleviated by a mask change at which time the metal overlap for the bottom plate interconnection was also changed. This change allowed for a greater overlap of metal I for the bottom capacitor plate connection and the metal II interconnect. The bigger problem of etching the interconnect metal was solved by double coating the photoresist to obtain a thicker layer.

In addition to the process problems discussed above, the fabrication of the capacitors presented several problems. To fabricate a good monolithic thin-film capacitor, one must have a good surface on which to deposit the capacitor and the dielectric must be pinhole free. The original processing sequence had to be changed because the monocarpic resistor technique was causing the surface of the SiO_2 to become damaged. The result was that aluminum left in the pinholes in the SiO_2 surface caused a buildup of the bottom plate aluminum. This in turn lead to shorted capacitors.

Although this problem was alleviated by changing the process sequence, a more serious problem of dielectric definition existed. Originally, a monocarpic copper film was used to define the SiO dielectric area. However, this technique left either small particles of copper on the bottom capacitor plate causing shorts, or in removing the copper, part of the bottom plate was removed. The reason for this problem was the adhesion between the copper and aluminum. Although considerable effort was spent in solving this problem, it was finally circumvented by utilizing a mechanical mask for the dielectric deposition. Since the dielectric is deposited in one large area for all capacitors, the mask is easily aligned and the resulting dielectric was free of pinholes and defects.

5.2 CIRCUIT PERFORMANCE PROBLEM AREAS

The two basic performance problems were a low-carrier frequency and low-signal strength. The low-carrier frequency resulted from several effects. First was a parasitic capacitance which appeared in parallel with the tank capacitor. This parasitic is primarily caused by capacitance between the bottom plates of C_1 and C_2 shown in Figures 3 and 21 and the bottom plate of the tank capacitor C_3. The SiO_2 passivation layer acts as the dielectric while the epitaxial layer acts as the bottom plate of this parasitic capacitance. Although this problem cannot be completely alleviated, it can be reduced by providing a thicker SiO_2 passivation layer.

The low-signal strength of the NRO-01 ($\simeq 75$ μV) was due primarily to f_t of the monolithic transistors at the operating bias level. Each half of the oscillator draws approximately 0.5 mA. The f_t of these devices is reduced considerably while operating at this level. Since stability and running time were typically four times better than the requirements, higher bias currents can be tolerated to increase the f_t. This has been tried by trimming the regulator resistors and found to exhibit the desired results. In future circuits, a change in the resistor mask should be made to accomplish the desired effect.

6. RECOMMENDATIONS

The research, development, and manufacture of an integrated circuit telemetry oscillator has yielded a sophisticated and reproducible device. However, additional work should be accomplished in two areas. The first area is the temperature performance of the regulator circuit. An investigation should be made into a redesign of the regulator not only to improve existing performance but also evaluate the possibility of the regulator compensating the TCF of the oscillator. This might be accomplished with the existing design by changing only the resistor and interconnect metallization patterns. The second area in which additional work should be accomplished is the resistance modulated device. The gain stage in the resistance modulator should be modified to decrease the gain and, therefore, decrease sensitivity to bias currents. Again, this task can probably be accomplished without major redesign of the basic monolith. It is, therefore, recommended that these two tasks be undertaken to realize the full versatility of this device.

APPENDIX A
TEST FIXTURE DESIGN

To test the NRO circuit to the design goals, it was necessary to design and fabricate two special test fixtures. The first test fixture is shown in Figure A-1. Basically, it performs the frequency-time measurement on the oscillator by cycling the B+ voltage off and on. The period and pulsewidth can be continuously varied from 10 msec to 2 sec. This fixture, in conjunction with a receiver and oscilloscope, displays the characteristic frequency-time performance shown in Figure 24.

The test fixture schematic shown in Figure A-2 was designed and used to test the resistance modulator circuit. A 6-V lamp is used as the heat source for the temperature transducer. The amount of heat is controlled by the voltage applied to the lamp. To control the heat transfer to the transducer, a timing circuit activates a shutter across the lamp and triggers an oscilloscope. The characteristic shown in Figure 10 illustrates the type of information achieved with this test circuit.

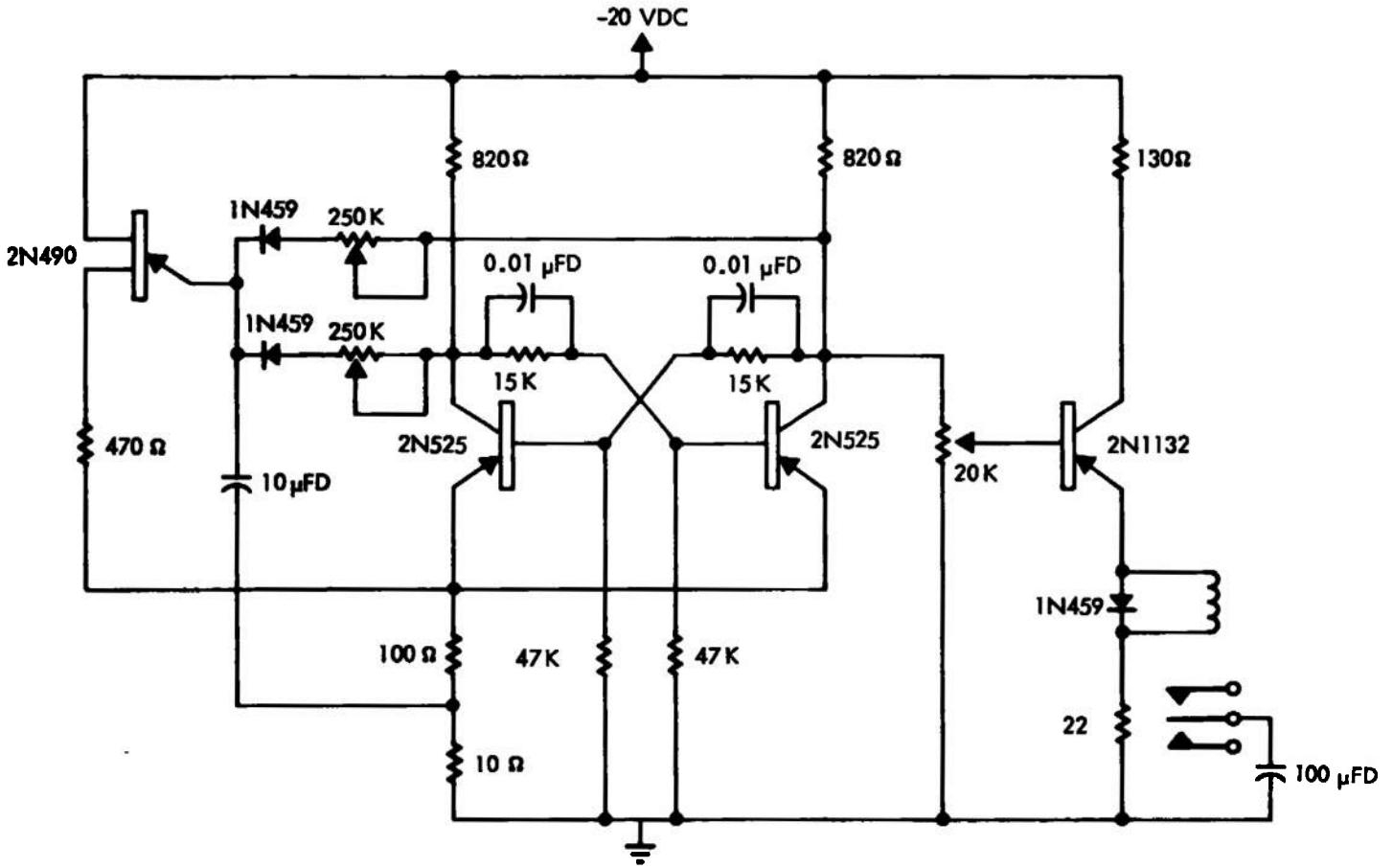
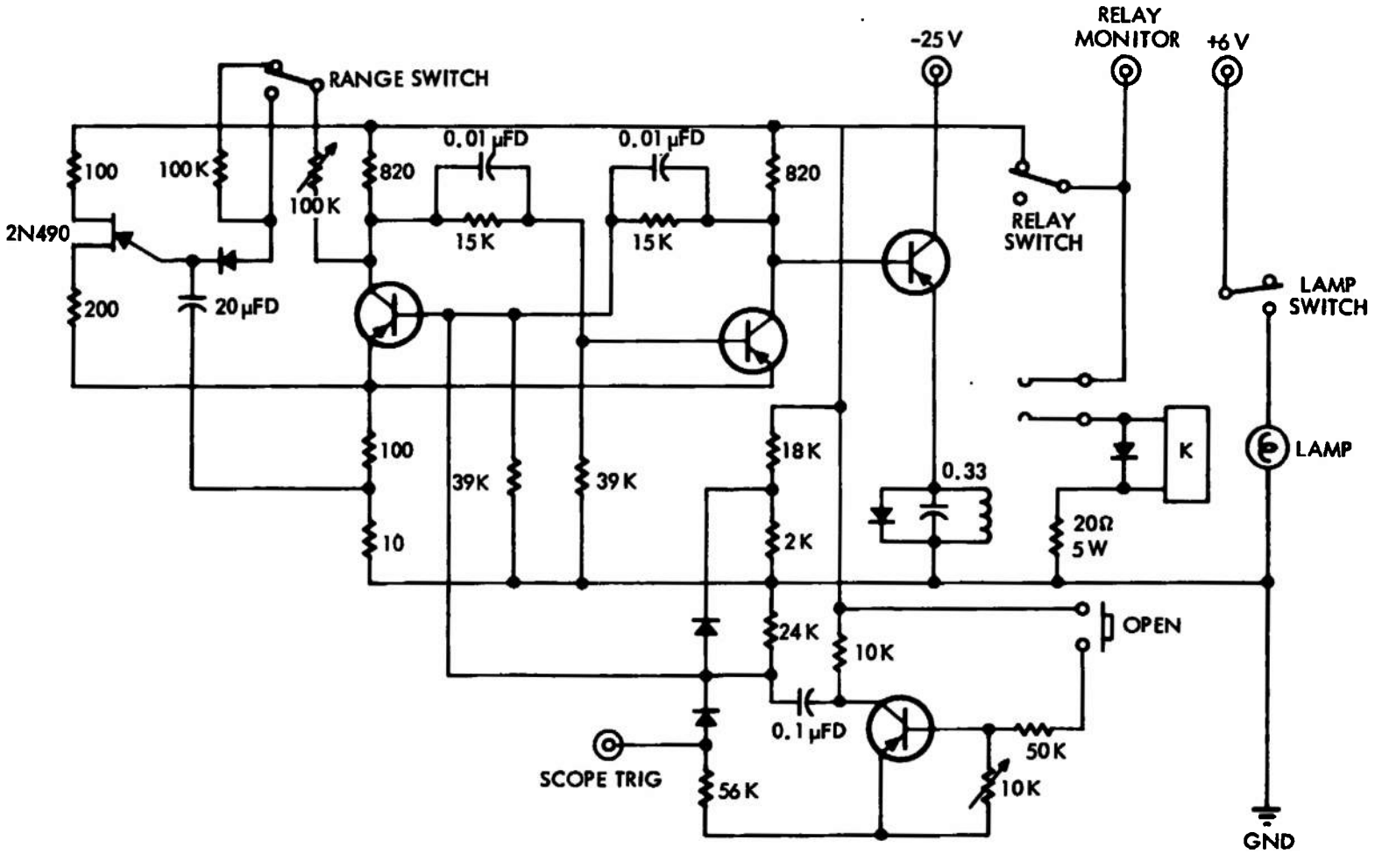


Figure A-1. Frequency-Time Test Circuit



NOTE:

1. ALL DIODES ARE SILICON GENERAL PURPOSE TYPE
2. ALL RESISTORS ARE 1/2 WATT UNLESS OTHERWISE SPECIFIED
3. ALL TRANSISTORS ARE 2N1132 UNLESS OTHERWISE SPECIFIED

Figure A-2. Resistance Modulator Test Circuit

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13. ABSTRACT

The design of a hybrid microminiaturized telemetry unit for use in gun launched projectiles is described. High peak accelerations during launch and short duration flight (2 milliseconds) were two prime considerations during design. The unit was designed and tested at Arnold Engineering Development Center in Ranges K and G of the von Kármán Gas Dynamics Facility. Initial tests indicated that this type of fm telemetry in the 150 mc frequency range would be feasible for aerodynamic measurements.

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